AMENDMENT TO THE CLAIMS

The following is a detailed listing of all claims that are, or were, in the Application.

1. (Previously presented) A multi-chip module (MCM) comprising:

a first integrated circuit (IC) chip on a substrate;

a first ground plane coupled to the first IC chip;

a second IC chip on the substrate; and

a second ground plane coupled to the second IC chip;

wherein the first ground plane is physically separated and electrically isolated from the second ground plane.

2. (Original) The MCM of Claim 1, wherein each of the first and second ground planes is coupled to at least one external lead of the MCM.

3. (Original) The MCM of Claim 1, wherein each of the first and second ground planes is formed as a respective trace on the substrate.

4. (Original) The MCM of Claim 1, wherein each of the first and second ground planes is substantially rigid.

5. (Original) The MCM of Claim 1, wherein each of the first and second ground planes is substantially flexible.

6. (Original) The MCM of Claim 1, wherein each of the first and second ground planes comprises a strip of conductive material.

7. (Original) The MCM of Claim 1, wherein each of the first and second ground planes comprises a layer of conductive material.

8. (Original) The MCM of Claim 1, wherein each of the first and second ground planes comprises a substantially solid layer of conductive material.

9. (Original) The MCM of Claim 1, wherein each of the first and second ground planes comprises a grid of conductive material.

10. (Original) The MCM of Claim 1, wherein the first chip is bonded to the first ground plane, and the second chip is bonded to the second ground plane.

11. (Original) The MCM of Claim 1, wherein the first chip is attached to the first ground plane, and the second chip is attached to the second ground plane.

12. (Original) The MCM of Claim 1, wherein at least one of the first and second chip comprises a dynamic random access memory (DRAM) chip.

13. (Original) The MCM of Claim 12, wherein the first and second chips are attached to the first and second ground planes via a flip-chip technique.

14. (Original) The MCM of Claim 1, wherein at least one of the first and second chips comprises a memory chip.

15. (Original) The MCM of Claim 1, wherein at least one of the first and second chip comprises an application specific integrated circuit (ASIC).

16. (Original) The MCM of Claim 1, wherein one of the first and second chips is coupled to a plurality of input/output connectors of the MCM and the other of the first and second chips is not coupled to any input/output connectors of the MCM.

17. (Original) The MCM of Claim 1, wherein the first chip is coupled to the second chip via at least one trace.

18. (Original) The MCM of Claim 1, wherein at least one of the first and second chips may be tested without affecting operation of the other of the first and second chips in the MCM.

19. (Original) The MCM of Claim 1, wherein at least one of the first and second chips may be tested without being affected by an operation of one or more other chips in the MCM.

20. (Original) The MCM of Claim 1, further comprising:

a first power plane coupled to the first IC chip; and

a second power plane couple to the second IC chip.

21. (Withdrawn) A method of testing first and second integrated circuit (IC) chips on a substrate in a multi-chip module, the first IC chip provided with a first ground plane and the second IC chip provided with a second ground plane, the method comprising:

testing the first IC chip without affecting an operation of the second IC chip; and

testing the second IC chip without affecting an operation of the first IC chip.

22. (Withdrawn) A method of testing first and second integrated circuit (IC) chips on a substrate in a multi-chip module, the first IC chip provided with a first ground plane and the second IC chip provided with a second ground plane, the method comprising:

testing the first IC chip without being affected by an operation of the second IC chip; and

testing the second IC chip without being affected by an operation of the first IC chip.

23. (Withdrawn) A method of testing at least one interconnect between two integrated circuit (IC) chips on a substrate in a multi-chip module, the first IC chip provided with a first ground plane and the second IC chip provided with a second ground plane, the method comprising:

applying a signal to the first IC chip; and

determining a current change on the interconnect in response to the signal applied to the first IC chip.

24. (Withdrawn) A method of making a multi-chip module (MCM) comprising:

providing a substrate;

providing a first ground plane and a second ground plane on the substrate; and

providing a first integrated circuit (IC) chip for the first ground plane and a second IC chip for the second ground plane.

25. (Withdrawn) The method of Claim 24 comprising providing a first power plane for the first chip and a second power plane for the second chip.

26. (Withdrawn) The method of Claim 24 comprising attaching the first and second ground planes to the substrate.

27. (Withdrawn) The method of Claim 26, wherein testing the first IC chip comprises supplying power to the first IC chip without supplying power to the second IC chip.

28. (Withdrawn) The method of Claim 26 comprising attaching the first and second chips to the substrate.

29. (Withdrawn) The method of Claim 24, wherein testing the first IC chip comprises supplying power to the first IC chip without supplying power to the second IC chip.

30. (Withdrawn) The MCM of Claim 29, wherein the first power plane supports a first voltage level and the second power plane supports a second power level.

31. (Withdrawn) The MCM of Claim 29, further comprising a third power plane coupled to both first and second IC chips.